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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/816,503	04/01/2004	Hong-Jyh Li	2004P51130US/I331.128.101	8623

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Dicke, Billig & Czaja, PLLC
Suite 2250
Fifth Street Towers
100 South Fifth Street
Minneapolis, MN 55402

EXAMINER	
JOHNSTON, PHILLIP A	

ART UNIT	PAPER NUMBER
2881	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/816,503	LI, HONG-JYH	
	Examiner	Art Unit	
	PHILLIP A. JOHNSTON	2881	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 February 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,4-9,12-25 and 28-31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,4-9,12-25 and 28-31* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Detailed Action

1. This Office Action is submitted in response to the RCE/Amendment filed 2-29-2008, claims 1, 8, 16, and 25 have been amended, and claims 3, 11, and 27 have been cancelled. Claims 1, 4-9, 12-25, and 28-31 are pending.

Claims Rejection – 35 U.S.C. 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which the subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,995,079 to Koezuka, in view of Jeon, U.S. Patent No. 6,790,755.

4. Regarding claim 1, Koezuka teaches an ion implantation apparatus at Col. 3, line 21-40, as shown below in Figure 2 having the following claimed elements;

(a) Vacuum chamber 102,

(b) Vacuum pumping system 106,

(c) Gas supplied from tanks 110-112.,

(d) Plasma ion source 101,

(e) Dopant ions produced from Group 2, 3, 5, and 6 elements; e.g. B, Al, Ga, In, and Zn, are supplied from tanks 110 and 111,

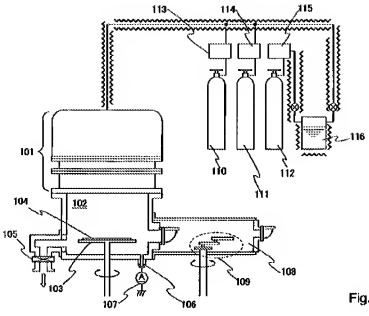

Fig. 2

(f) Plural power supplies (voltage sources) to ionize the gas and accelerate the resultant ions, via a bias applied to the substrate 104. See also Col. 7, line 11-16.

(g) Wafer support stage 103,

5. Koezuka fails to disclose implanting ions into a high-k dielectric layer having a k value greater than 9.

6. Jeon teaches ion implantation after deposition of alternating sub-layers of high-k dielectric and areard-k dielectric materials on a semiconductor substrate. The high-K dielectric materials have a K value of about 20 or more. Such high-K dielectric materials include, for example, HfO_2, ZrO_2, and Ta2 O_5. Col. 4, line 1-10; and Col. 14, line 9-20.

7. Jeon modifies Koezuka to provide nitridation of high-k dielectric layers to produce semiconductor devices having the electrical advantages of a higher K.

8. Therefore it would have been obvious to one of ordinary skill in the art that the plasma reactor apparatus of Koezuka can be modified to use ion implantation of high-k layers in accordance with Jeon, to provide a semiconductor device having a composite dielectric layer, where the composite dielectric layer is formed about the boundary of each first dielectric material layer/second dielectric material layer.

9. Claims 4-9, 12, 16-25, 28, and 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over USPN 6,995,079 to Koezuka, in view of Jeon, USPN 6,790,755, and in further view of USPN 6,518,195 to Collins.

10. Regarding claims 8, 12, and 16, the combination of Koezuka and Jeon discloses all the claimed limitations as described above regarding claim1, but fails to teach the use of a constant DC voltage supply for accelerating positive ions and repelling negative ions.

11. Collins discloses the use of AC supply 31 and DC supply 42 provides a constant positive or negative DC bias between the sample holder and the chamber wall (Col. 11, line 60-67), where a negative bias extracts positive ions toward (accelerate) the wafer.

One of ordinary skill in the implantation art recognizes that applying a negative bias to the sample would repel negative ions.

Therefore it would have been obvious to one of ordinary skill in the art that the ion implantation apparatus of Koezuka and Jeon, would use the AC and DC voltage sources of Collins to accelerate ions from the plasma to impinge on the wafer in order to control implantation of the ions.

12. Regarding claims 4, 5, and 9, the combination of Koezuka, Jeon, and Collins discloses the DC and AC voltage sources as described above regarding claim 8.

13. Regarding claim 6, Koezuka teaches vacuum pumping system 106 at Col. 3, line 21-28.

14. Regarding claim 7, Koezuka teaches gas supply and flow control at Col. 3, line 32-40.

15. Regarding claims 25, 28, and 29, the combination of Koezuka, Jeon, and Collins discloses the apparatus used in these method claims, as described above regarding claims 4, 5, and 8.

16. Claims13-15, are rejected under 35 U.S.C. 103(a) as being unpatentable over USPN 6,995,079 to Koezuka, in view of Jeon, USPN 6,790,755, in further view of USPN 6,518,195 to Collins, and in still further view of USPN 2001/0054746 to Yamada.

17. Regarding claims 13-15 the combination of Koezuka, Jeon, and Collins teaches all the limitations therein as described above regarding claim 1, but fails to teach the use of a buffer layer.

18. Yamada teaches a buffer layer 6 such as amorphous silicon or epitaxially grown single crystal silicon, silicides, or metals, or insulating films of BSG (boron silicate glass), where the silicide or the metal particularly contributes to decreasing the resistance of the external base. See [0128] and [0141].

19. Yamada modifies Koezuka, Jeon, and Collins to provide a method for making a silicide buffer layer, where a metal such as titanium (Ti) or cobalt (Co) stacked by

sputtering, for example, is annealed by RTA (rapid thermal annealing) for a short time to make the metal and silicon react forming TiSi. [0161]

20. Therefore it would have been obvious to one of ordinary skill to provide plural buffer layers on silicide stacks that include metals such as titanium (Ti) or cobalt (Co), and implanting ions in the buffer layers to adjust doping levels.

21. Regarding claim 17, Koezuka discloses forming a device having a plurality of insulating and conductive layers at Col. 6, line 32-48; and implanting ions into the plural layers at Col. 7, line 24-61, which would also include the use of adjacent high-k dielectric layers as described above regarding claim 1.

22. Regarding claims 18, and 19 the combination of Koezuka and Jeon teaches all the limitations therein as pointed out above regarding claims 1,16, and 17.

23. Regarding claims 20-22, the combination of Koezuka, Jeon, Collins and Yamada teaches the use of a buffer layer, as described above regarding claims 13-15.

24. Regarding claims 23 and 24, the combination of Koezuka, Jeon, Collins and Yamada teaches the voltage sources, as described above regarding claims 13-16.

25. Regarding claim 30, Koezuka discloses implant dose rates between 10^{13} and 10^{16} at Col. 7, line 27-34.

26. Claim 31 is rejected under 35 U.S.C. 103(a) as being unpatentable over USPN 6,995,079 to Koezuka, in view of Jeon, USPN 6,790,755, in further view of USPN 6,518,195 to Collins, and in still further view of USPN 6,248,662 to Wu.

27. Regarding claim 31, the combination of Koezuka, Jeon, and Collins fails to teach implanting ions with an energy range of 5-10 kev.

28. Wu teaches the use of an ion implantation sources where BF3 ions are implanted at a typical energy of about 5.0 KeV. Col. 3, line 5-17.

29. Wu modifies Koezuka and Jeon to provide an ion source where the energy of the implanted ions is restricted so that the implanted ions are only concentrated in the surface of the first dielectric layer.

30. Therefore it would have been obvious to one of ordinary skill to implant ions at energies that have been selected to form void-free dielectric layers.

Conclusion

31. Any inquiry concerning this communication or earlier communications should be directed to Phillip Johnston whose telephone number is (571) 272-2475. The examiner can normally be reached on Monday-Friday from 7:00 am to 4:00 pm. If attempts to reach the examiner by telephone are unsuccessful, the examiners supervisor Robert Kim can be reached at (571)272-2293. The fax phone number for the organization where the application or proceeding is assigned is 571 273 8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should

you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

PJ

May 23, 2008

/ROBERT KIM/

Supervisory Patent Examiner, Art Unit 2881